REMARKS

Summary of the Office Action

Claims 1-40 and 42-71, and 73-127 were pending in this application.

Claims 122-127 are allowed.

Claims 1-39 are rejected under 35 U.S.C. § 102(b) as being anticipated by Azaren et al., U.S. Patent No. 5,357,249 (hereinafter "Azaren"). Claims 40, 42-71, and 73-101 are rejected under 35 U.S.C. § 102(e) as being anticipated by Johansen et al., U.S. Patent No. 6,631,144 (hereinafter "Johansen"). Claims 102-121 are rejected under 35 U.S.C. § 102(b) as being anticipated by Ariyavisitakul et al., U.S. Patent No. 5,084,891 (hereinafter "Ariyavisitakul").

Summary of Applicants' Reply

Applicants appreciate the allowance of claims 122-127.

Applicants have amended claims 1, 26, 40, 71, 102, and 112 to more particularly define the invention. No new matter has been added and the amendments are fully supported and justified by the specification. Applicants have canceled claim 31 without prejudice.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Applicants' Reply to the Rejection of Claims 1-25 under 35 U.S.C. § 102(b)

The Examiner rejected claims 1-39 under 35 U.S.C. § 102(b) as being anticipated by Azaren. This rejection is respectfully traversed.

Applicants' amended independent claim 1 is directed toward an apparatus for receiving and processing a clock data recovery (CDR) signal. The apparatus contains a programmable logic device (PLD) and processing circuitry at least partly controlled by the PLD circuitry. First input circuitry is configured to receive the CDR signal which includes data information and a clock signal embedded in a serial data stream. Second input circuitry is configured to receive an external reference clock signal which has a frequency related to the frequency of the embedded clock signal. The processing circuitry is configured to use the external reference clock signal to recover the data information from the CDR signal.

Azaren refers to an apparatus that receives a serial optical digital data signal and converts the signal to a parallel electrical digital data signal. As shown in FIG. 2 of Azaren, the receiver board 36 receives serial data

signal 38 as well as an external reference clock signal (EXTERNAL SCLK INPUT). However, the data information embedded in the serial data signal (LDATA) is recovered from the serial data signal without using the external reference clock signal.

In fact, the external reference clock signal is not even supplied to clock/data recovery circuit 44. Instead, the external reference clock signal is only supplied to OCON ASIC 46, where one of the external reference clock signal or the internally generated clock is selected to synchronize the parallel data output (See, e.g., FIG. 9, elements 104 and 124). Thus, Azaren fails to show recovering the data information from the CDR signal using the external reference clock signal, as required by applicants' amended independent claim 1.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Applicants' Reply to the Rejection of
Claims 26-30 and 32-39 under 35 U.S.C. § 102(b)

The Examiner rejected claims 26-39 under 35 U.S.C. § 102(b) as being anticipated by Azaren. This rejection is respectfully traversed.

Applicants' amended independent claim 26 is directed toward an apparatus for producing and transmitting a clock data recovery (CDR) signal. The apparatus contains a programmable logic device (PLD) configured to produce data information and a PLD clock signal. Input circuitry is configured to receive an external reference clock signal. Buffer circuitry is configured to buffer the data information between the clock regime associated with the PLD clock signal and a different clock regime associated with the external reference clock signal, where the two clock regimes have different frequencies. Output circuitry is configured to use the reference clock signal to produce the CDR signal including the data information and an embedded clock signal having a frequency related to the external reference clock signal.

Azaren refers to an apparatus that receives a parallel electrical digital data signal and transmits a serial optical digital data signal based on the parallel data signal. As shown in FIG. 1 of Azaren, transmitter board 12 receives parallel data signals (DATA) as well as an external reference clock signal (EXTERNAL SCLK). Within ICON ASIC 14 (FIG. 4) the parallel data signals are buffered from the external reference clock regime to an internal sample rate clock regime. However, the "internal sample rate is the same

as the external sample clock" (Azaren, column 6, lines 24-25). Thus, Azaren does not show buffering the data information between two clock regimes having different frequencies, as required by applicants' amended independent claim 26.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 26 under 35 U.S.C. § 102(b) be withdrawn.

Claims 27-30 and 32-39 are dependent from claim 26 and are allowable at least because claim 26 is allowable.

Applicants' Reply to the Rejection of Claims 40, 42-71, and 73-101 under 35 U.S.C. § 102(e)

The Examiner rejected claims 40, 42-71, and 73-101 under 35 U.S.C. § 102(e) as being anticipated by Johansen. This rejection is respectfully traversed.

Applicants' amended independent claim 40 is directed toward an apparatus for receiving an information signal which includes data information having clock information for the data information embedded in the data information. The apparatus is configured to receive a programmable scale factor, the information signal and an external reference clock signal. The external reference clock signal is related to the frequency of the clock

information embedded in the data information by the programmable scale factor.

Applicants' amended independent claim 71 is directed toward an apparatus for transmitting an information signal which includes data information having clock information for the data information embedded in the data information. The apparatus is configured to receive a programmable scale factor and an external reference clock signal having a frequency related to the frequency of the clock information by the programmable scale factor. Reference clock signal processing circuitry is configured to use the external reference clock signal to produce a further reference clock signal having the frequency of the clock information. Data processing circuitry and data signal processing circuitry produce a data signal indicative of the data information and process the signal with the further reference clock signal to produce the information signal.

Johansen refers to a multi-rate transponder system having a receiving part and a transmitting part. The receiving part receives an incoming serial data stream and derives a clock signal and data signal from the incoming data stream. The transmitting part generates an outgoing data signal based on the internally generated reference clock signal. However, the system of Johansen does not show a

receiver or a transmitter having input circuitry operative to receive an external clock signal. Thus, Johansen fails to show receiving an external clock signal as required by applicants' amended independent claims 40 and 71.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claims 40 and 71 under 35 U.S.C. § 102(e) be withdrawn.

Claims 42-70 and 73-101 are dependent from claims 40 and 71 respectively and are allowable at least because claims 40 and 71 are allowable.

Applicants' Reply to the Rejection of
Claims 102-121 under 35 U.S.C. § 102(b)

The Examiner rejected claims 40, 42-71, and 73-101 under 35 U.S.C. § 102(b) as being anticipated by Ariyavisitakul. This rejection is respectfully traversed.

Applicants' amended independent claim 102 is directed toward programmable serializer circuitry. The programmable serializer circuitry contains control circuitry that receives a programmable number, input circuitry that received that programmable number of input signals in parallel, and output circuitry that produces an output signal that is serially indicative of the programmable number of input signals. For example, if the programmable serializer

receives "six" as the programmable number, then six-bit parallel words will be serialized.

Applicants' invention, as defined by amended independent claim 112, is directed toward programmable deserializer circuitry. The programmable deserializer circuitry contains control circuitry that receives a programmable number, input circuitry that receive an input signal that is serially indicative of plural bits of information one after another and stores the programmable number of successive ones of those bits, and output circuitry that produces the programmable number of parallel output signals indicative of the bits stored by the input circuitry. For example, if the programmable deserializer receives "six" as the programmable number, then the serial input will be deserialized into six-bit parallel words.

Ariyavisitakul refers to a technique for bit synchronization and error detection in a TDM/TDMA system that includes serializer and deserializer circuits. However, the serializer and deserializer of Ariyavisitakul are not programmable and are only capable of serializing and deserializing eight-bit words. Thus, Ariyavisitakul fails to show all of the elements required by applicants' amended independent claims 102 and 112.

Accordingly, for at least this reasons, applicants respectfully request that the rejection of claims 102 and 112 under 35 U.S.C. § 102(b) be withdrawn.

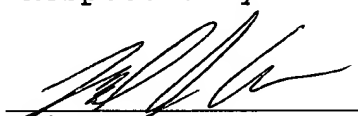
Claims 103-111 and 113-121 are dependent from claims 102 and 112 respectively and are allowable at least because claims 102 and 112 are allowable.

Conclusion

For at least the foregoing reasons, applicants respectfully submit that this application is in condition for allowance.

Accordingly, prompt reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,



Michael J. Chasan
Registration No. 54,026
Agent for Applicants
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 36981
1251 Avenue of the Americas
New York, New York 10020-1105
(212) 596-9000